**GOVERNMENT POLYTECHNIC**

**CHHAPRA**



COURSE FILE (Lecture Plan)

OF

**DIGITAL ELECTRONICS & MICROPROCESSOR (2018304)**

Faculty Name:

Prof. SAURAV KUMAR

Lecturer

**DEPARTMENT OF COMPUTER SCIENCE ENGINEERING**

|  |
| --- |
| **STATE BOARD OF TECHNICAL EDUCATION** |
| Bihar, PatnaSS.JPG&CC.JPG |

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Department of Computer Science Engineering

**Vision**

To contribute effectively to the important national endeavor to produce quality human resource in the information technology and related areas for sustainable development of the country's IT industry needs.

**Mission**

1. To ensure sufficient modern technological exposure to the students in order to create skilled professionals.

2. To frequently update the labs keeping in view the requirement of the current industry scenario.

3. To extend counseling and career guidance facility to the students to help them to achieve their goal.

4. To encourage faculties and staffs to pursue higher education and to do the research work.

5. To encourage faculties and staffs to participate in various seminars, conferences and workshops to keep themselves updated of the state-of-the-art technology.

**Course Description:-**

The subject will help the students to learn facts, concepts, principle and procedure of digital electronics. These techniques can be used for designing sequential and combinational circuits which forms the basis of any electronic device. Also, this subject is designed to give clear idea about working principles of 8085 microprocessor.

**Course Objectives: -**

The objective of this subject is to enable the students to know basic concepts of digital electronics and familiarity with available chips. After undergoing this course, the students will have the awareness of various arithmetic circuits, counter design, registers, A/D and D/A converters, semi-conductor memories, multiplexers and de-multiplexers etc

**Course Syllabus**

**CONSUMER ELECTRONICS (ELECTRONICS ENGINEERING GROUP)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Subject Code 2018304** | **Theory** |  | **Credits** |
| **No. of Periods Per Week** | **Full Marks** | **:** | **100** | **02** |
| **L** | **T** | **P/S** | **ESE** | **:** | **70** |
| **03** | **-** | **-** | **TA** | **:** | **10** |
| **-** | **-** | **-** | **CT** | **:** | **20** |

**Course Objectives:** The objective of this subject is to enable the students to know basic concepts of digital electronics and familiarity with available chips. After undergoing this course, the students will have the awareness of various arithmetic circuits, counter design, registers, A/D and D/A converters, semi-conductor memories, multiplexers and de-multiplexers etc.

|  |  |  |
| --- | --- | --- |
| **Contents: Theory** | Hrs. | Marks |
| **Unit – 1** | **NUMBER SYSTEM:**Decimal, binary, octal and hexadecimal, hexa-decimal number systems, Conversion from one system to another,1’s,2’s and 9’s,10’s complements signed numbers Codes: BCD, Excess-3, Gray codes weighted and non-weighted codes, binary arithmetic, | [6] |  |
| **Unit – 2** | **LOGIC GATES AND FLIP FLOPS:**Definitions, symbols and truth table of NOT, OR, AND, NAND, NOR, XOR, XNOR gates, basic gates, universal gates, De Morgan’s Theorems; Karnaugh-Map ,Sum of Product, Product of Sum, Min term , Max term, Logical diagram, truth table, Flip -Flops- RS, T, D, JK, Master/ Slave JKand timing diagram. | [8] |  |
| **Unit – 3** | **REGISTERS:**Shift Registers Serial in Serial out Serial in Parallel outParallel in Parallel outParallel in Serial out Bidirectional Shift Register | [5] |  |
| **Unit – 4** | **COUNTERS:**Asynchronous counters Synchronous CounterDecade counter and its application Cascade Counter, Encoder & Decoder | [6] |  |

|  |  |  |  |
| --- | --- | --- | --- |
| **Unit – 5** | **LOGIC FAMILY & CIRCUITS:**Digital integrated circuitsHalf adder and full adder circuit, Half Subtractor and full subtractor circuit, design and implementation, Multiplexer, Demultiplexer. | [6] |  |
| **Unit – 6** | **A/D AND D/A CONVERTERS:**Analog to digital convertor, Digital to Analog Convertor,ADC comparator, Dual Slope ADC, Successive ADC. | [8] |  |
| **Unit – 7** | **MEMORIES AND DISPLAY DEVICES:**Memory UnitConcept of memories using registers Primary MemorySecondary MemoryStatic and Dynamic MemoryLCD, LED, Seven Segment Display Basic operation and Applications, Dot Matrix display. | [6] |  |
| **Unit – 8** | **MICROPROCESSORS:**Evaluation of microprocessors, microcomputer organization,8085 architecture,8085 pin diagram 8085 flag register & timing diagram, instruction sets, addressing modes,8086 architectures, 8086 pin diagram, 8086 Flag register instruction setsand addressing modes | [5] |  |

**Text Books:**

1. Digital Electronics and Applications, McGraw Hills Publishers. - Malvino Leach
2. Digital Logic and Computer Design, Prentice Hall of India Ltd., New Delhi. - Morries Marrow
3. Digital Integrated Electronics, Prentice Hall of India Ltd., New Delhi - Herbert Raub and Donal Sachilling
4. Digital Electronics, Prentice Hall of India Ltd., New Delhi – Rajaraman
5. Microelectronics, McGraw Hill, 1987 - J. Millman and A. Grabel
6. Linear Integrated Circuits, Wiley Eastern, 1991 - D. Roychaudhuri and S.B. Jani

**References:**

1. Digital Principles, Latest Edition, 2000, Tata McGraw Hill Publishing Company Ltd., New Delhi - Malvin& Leach
2. Modern Digital Electronics, Second Edition, 2000, Tata McGraw Hill Publishing Company Ltd., New Delhi - R.P. Jain
3. Digital Electronics, First Edition, 2000, Tata McGraw Hill Publishing Company Ltd., New Delhi - V.K. Puri
4. Electronics Circuits and Systems, 1992, Tata McGraw Hill Publishing Company - Y.N. Bapat
5. Modern Digital Electronics, 1983, Tata McGraw Hill Publishing Company - R.P. Jain
6. Digital Computer Fundamentals, T.M.H. - Malvino
7. Digital Computer, Dhanpat Roy & Sons. - B. Ram
8. Introduction to Microprocessors, Dhanpat Roy & Sons. - Dr. B. Ram

**Course outcomes:**

1. Define basic logical circuits, Boolean algebra, minimization methods, methods for writing Boolean functions, combinational and sequential circuits, flip-flops, digital automaton, programmable structures
2. Describe operation methods of combinational and sequential circuits, similarities and differences of writing the Boolean functions and minimizations
3. Select appropriate methods for realization and circuit minimization
4. Pattern recognition for specific circuit realization and error discovery during circuit design process
5. Synthesis of appropriate combinational and sequential logic circuits
6. Evaluation of own solutions and error discovery

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**TIME TABLE**

**FACULTY: -** Prof. Saurav Kumar (Electronics Engineering Department)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | 1st10:00-11:00 | 2nd1:00-12:00 | 3rd12:00-1:00 |  | 4th2:00-3:00 | 5th3:00-4:00 | 6th4:00-5:00 |
| MON |  |  | **Digital Electronics & Microprocessor (2018304) (Saurav)** | LUNCH |  |  |  |
| TUE |  |  | **Digital Electronics & Microprocessor (2018304) (Saurav)** |  |  |  |
| WED |  |  | **Digital Electronics & Microprocessor (2018304) (Saurav)** |  |  |  |
| THU |  |  |  |  |  |  |
| FRI |  |  |  |  |  |  |
| SAT |  |  |  |  |  |  |

**GOVERNMENT POLYTECHNIC CHAPRA**

**CLASS ROUTINE FOR DIPLOMA 3rd SEMESTER CS- Computer Science Engineering**

**Student list**

**Computer Science Engineering.**

|  |
| --- |
| **Branch-Computer Sc.& Engg.** |
| **Subject-** |
| **Roll Number** | **Name Of the Student** |
| 311131821001 | ANU KUMARI |
| 311131821002 | VINAY KUMAR |
| 311131821003 | RANU KUMAR |
| 311131821004 | ABHIMANYU KUMAR |
| 311131821005 | AARYAN KUMAR |
| 311131821006 | ANKIT KUMAR |
| 311131821008 | SACHCHIDANAND KUMAR |
| 311131821010 | MUKESH KUMAR RAY |
| 311131821012 | ANKIT KUMAR |
| 311131821013 | PRIY RANJAN |
| 311131821014 | AAKASH KUMAR |
| 311131821015 | AMAN KUMAR |
| 311131821016 | PRIYANKA KUMARI |
| 311131821018 | ASHISH RANJAN CHAUDHARI |
| 311131821019 | DHIRAJ KUMAR |
| 311131821020 | PREM KUMAR SAH |
| 311131821021 | GITANJALI MONI |
| 311131821023 | SANDEEP KUMAR |
| 311131821024 | VISHAL RAY |
| 311131821025 | ROHIT KUMAR |
| 311131821026 | SONU KUMAR |
| 311131821301 | ABHISHEK KUMAR CHOUBEY |

**LECTURE PLAN**

|  |  |
| --- | --- |
| **Topics** | **Lecture Number** |
| **NUMBER SYSTEM:** | **01-6** |
| Decimal, binary, octal and hexadecimal, hexa-decimal number systems, Conversion from one system to another | 1-2 |
| 1’s,2’s and 9’s,10’s complements | 3 |
| Signed numbers Codes: BCD, Excess-3 | 4 |
| Gray codes weighted and non-weighted codes | 5 |
| binary arithmetic | 6 |
| **LOGIC GATES AND FLIP FLOPS:** | **7-14** |
| Definitions, symbols and truth table of NOT, OR, AND, NAND, NOR, XOR, XNOR gates, basic gates, universal gates | 7-8 |
| De Morgan’s Theorems | 9 |
| Karnaugh-Map | 10 |
| Sum of Product, Product of Sum, Min term, Max term, Logical diagram, truth table | 11-12 |
| Flip -Flops- RS, T, D, JK, Master/ Slave JK and timing diagram. | 13-14 |
| **REGISTERS:** | **15-19** |
| Shift Registers, Serial in Serial out | 15 |
| Serial in Parallel out | 16 |
| Parallel in Parallel out | 17 |
| Parallel in Serial out | 18 |
| Bidirectional Shift Register | 19 |
| **COUNTERS:** | **20-25** |
| Asynchronous counters | 20 |
| Synchronous Counter | 21 |
| Decade counter and its application | 22 |
| Cascade Counter | 23 |
| Encoder  | 24 |
| Decoder | 25 |
| **LOGIC FAMILY & CIRCUITS:** | **26-31** |
| Digital integrated circuits | 26-27 |
| Half adder and full adder circuit | 28 |
| Half Subtractor and full subtractor circuit | 29 |
| Design and implementation | 30 |
| Multiplexer, demultiplexer | 31 |
| **A/D AND D/A CONVERTERS:** | **32-39** |
| Analog to Digital convertor | 32-33 |
|  |  |
| Digital to Analog Convertor | 34-35 |
| ADC comparator | 36-37 |
| Dual slope ADC | 38 |
| Successive ADC | 39 |
| **MEMORIES AND DISPLAY DEVICES:** | **40-45** |
| Memory Unit, Concept of Memories Using Registers | 40 |
| Primary Memory, Secondary Memory | 41 |
| Static And Dynamic Memory | 42 |
| LCD, LED, Seven Segment Display43 | 43 |
| Basic Operation and Applications | 44 |
| Dot Matrix Display | 45 |
| **MICROPROCESSORS:** | **46-50** |
| Evaluation of microprocessors, microcomputer organization | 46 |
| 8085 architectures | 47 |
| 8085 pin diagram 8085 flag register & timing diagram, instruction sets, addressing modes | 48 |
| 8086 architectures | 49 |
| 8086 pin diagrams, 8086 Flag register instruction setsand addressing modes | 50 |

**This document is approved by**

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| --- | --- | --- |
| **Designation** | **Name** | **Signature** |
| Course Coordinator | Prof. Saurav Kumar |  |
| HoD | Prof. Om Prakash Aditya |  |
| Principal | Dr. Anil Kumar Singh |  |
| Date |  |  |